

REMARKS

Applicants have amended the title of the above-identified application, pursuant to the requirement by the Examiner in Item 1 on page 2 of the Office Action mailed April 8, 2004, to provide a title more clearly indicative of the presently claimed invention. In view of this amended title, the requirement therefor has been satisfied.

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 1 to recite that the wiring substrate has a periphery, in addition to, inter alia, the plurality of chip mounting areas; to recite that the plurality of chip mounting areas are arranged in a matrix formation of a rectangular shape having opposed longer sides and opposed shorter sides; and to recite, in (d) sealing the plurality of semiconductor chips, that this sealing is performed by a transfer molding such that the resin member is provided from one of the longer sides of the rectangular shape toward the other of the longer sides of the rectangular shape of the matrix formation, via plural flow gates positioned at the periphery of the wiring substrate. Note, for example, Fig. 15 of Applicants' original disclosure, together with, for example, the description in connection therewith on pages 24 and 25 of Applicants' specification. See also Fig. 16 of Applicants' original disclosure, and the corresponding description on page 25 of Applicants' specification.

Moreover, Applicants are canceling claim 7 without prejudice or disclaimer.

In addition, Applicants are adding new claims 8-10 to the application. Claims 8 and 9, dependent respectively on claims 1 and 8, respectively recites that the matrix formation includes groups of chip mounting areas clustered with each other, with the resin member being provided from one of the longer sides to a location

among a respective group of chip mounting areas, and distributed from this location to the chip mounting areas of the respective group of chip mounting areas; and recites that each group of chip mounting areas includes four chip mounting areas, with the location being among these four chip mounting areas. Claim 10, dependent on claim 1, recites that the wiring substrate includes a plurality of wiring substrate members distributed along the direction of the longer sides of the rectangular shape of the matrix formation, with each wiring substrate member having a respective group of chip mounting areas clustered with each other.

In connection with the newly added claims, note, for example, Figs. 15 and 16 of Applicants' original disclosure.

Applicants respectively submit that all of the claims now presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed April 8, 2004, that is, the teachings of the U.S. patents to Glenn, No. 6,150,193, to Lee, et al., No. 6,054,338, and to Mullen, et al., No. 5,241,133, under the provisions of 35 USC §102 and 35 USC §103.

It is respectfully submitted that these references as applied by the Examiner would have neither taught nor would have suggested such a method of manufacturing a semiconductor device as in the present claims, including, in particular, wherein the plurality of chip mounting areas of the wiring substrate are arranged in a matrix formation of a rectangular shape having opposed longer sides and opposed shorter sides; and wherein the sealing of the plurality of semiconductor chips, bonding wirings and first surface of the wiring substrate is performed by a transfer molding such that the resin member is provided from one of the longer sides of the rectangular shape toward the other of the longer sides of the rectangular

shape of the matrix formation, by way of plural flow gates positioned at the periphery of the wiring substrate. See claim 1.

In addition, it is respectfully submitted that the teachings of these applied references do not disclose, nor would have suggested, such a method of manufacturing a semiconductor package as in the present claims, having features as discussed previously in connection with claim 1, and, additionally, including (but not limited to) wherein the matrix formation includes groups of chip mounting areas clustered with each other, the resin member being provided from one of the longer sides to a location among a respective group of chip mounting areas and distributed from this location to each chip mounting area of this respective group of chip mounting areas (see claim 8), particularly wherein each group of chip mounting areas includes four chip mounting areas, the location from which the resin member is provided being among the four chip mounting areas (see claim 9); and/or wherein the wiring substrate includes a plurality of members distributed along the direction of the longer sides of the rectangular shape of the matrix formation, each wiring substrate member having a respective group of chip mounting areas clustered with each other (see claim 10); and/or wherein the wiring substrate includes a flexible tape substrate (see claim 2), especially wherein this flexible tape substrate includes a polyimide tape (see claim 3); and/or wherein the flexible tape substrate includes a plurality of through holes, with portions of the plurality of conductive layers arranged to cover the plurality of through holes, and with the plurality of bump electrodes being formed at the plurality of through holes so as to contact with the portions of the plurality of conductive layers (see claim 4), particularly wherein the plurality of bump electrodes are solder bump electrodes (see claim 5); and/or wherein the mounting of the plurality of semiconductor chips includes fixing each of the chips on the first

surface of the wiring substrate by an insulating adhesive layer respectively (see claim 6).

The present invention is directed to a technique for manufacturing a semiconductor package, particularly effective in connection with forming a packaged device having a base substrate that includes a flexible film. Applicants have found that by providing a sealing member for sealing the semiconductor chips, the bonding wires and the first surface of the wiring substrate as in the present claims, the required time for resin injection in sealing the structure by the resin member can be shortened, and a uniform resin injection can be achieved, so that total cost for assembling the packaged device can be reduced and uniformity of quality of the packaged device can be increased.

Specifically, Applicants have found that by performing the sealing using a transfer molding, and particularly wherein such transfer molding is performed using plural flow gates positioned at the periphery of the wiring substrate, with the resin being introduced from one of the longer sides of the rectangular shape toward the other of the longer sides, advantages set forth previously, of reduced time for resin injection and improved uniformity of resin injection, are achieved.

Glenn discloses a method of packaging an integrated circuit chip, the packaging including an electrically conductive shield layer including a cured flowable electrically conductive layer formed above an encapsulant layer. The shielding layer includes benefits as described, for example, at column 1, lines 25-34 of Glenn. The disclosed method includes steps of providing an insulated substrate having sections; mounting integrated circuit chips in the sections; and then encapsulating an insulating encapsulant layer. A conductive shield layer is then applied above the encapsulant layer, the shield layer including a flowable electrically conductive

material. The encapsulant layer, shield layer and insulating substrate are then cut along a periphery of each of the sections to form a plurality of shielded packages. See column 2, lines 50-59. Note also Fig. 7A and the description in connection therewith at column 7, lines 36-53, showing a substrate 13 which is preferably a square or rectangular substrate and will have a plurality of chips respectively provided thereon. This patent discloses that a layer of encapsulant 42 (see Figs. 11 and 12) is applied by partially filling a pocket defined by dam 59 with an electrically insulating liquid encapsulant. See column 10, lines 23-26. Note also column 9, lines 59-67, together with Fig. 11.

It is respectfully submitted that Glenn does not disclose, nor would have suggested, formation of the encapsulant by transfer molding, much less the specific transfer molding as in the present claims. Clearly, Glenn would have neither taught nor would have suggested the presently claimed subject matter.

Lee, et al. discloses a ball grid array (BGA) device and method of fabrication thereof, wherein a panel (for example, a bismaleimide triazine (BT) or ceramic) of substrate material is provided; and after providing an integrated circuit chip and wire bonds thereon, the chip and wire bonds are covered by encapsulating material 32 (see Fig. 3) as is well known. Note the paragraph bridging columns 2 and 3 of this patent.

It is respectfully submitted that Lee, et al. discloses a substrate upon which plural BGA devices are provided. It is respectfully submitted that this reference does not disclose, nor would have suggested, the sealing as in the present claims, being performed by a transfer molding, much less that the sealing is performed by a transfer molding such that the resin member is provided from one of the longer sides of the rectangular shape of the matrix formation of the plurality of chip

mounting areas, toward the other of the longer sides of the rectangular shape of the matrix formation, via plural flow gates positioned at the periphery of the wiring substrate, and advantages thereof as discussed in the foregoing.

It is respectfully submitted that the teachings of Mullen, et al. would not have rectified the deficiencies of either of Glenn or Lee, et al., such that the presently claimed invention as a whole would have been obvious to one of ordinary skill in the art.

Mullen, et al. discloses transfer molded leadless semiconductor packages. This patent discloses use of a resinous circuit carrying substrate having an array of solder pads on the bottom side and a semiconductor device electrically and mechanically mounted on the top side, with a protective plastic cover being transfer molded about the semiconductor device, covering substantially all of the top side of the circuit carrying substrate. See column 2, lines 35-42. Note also column 3, lines 19-30, describing various techniques for molding the protective plastic cover.

Even assuming, arguendo, that the teachings of Mullen, et al. were properly combinable with the teachings of either of Glenn or Lee, et al., such combined teachings would have neither disclosed nor would have suggested the presently claimed method, including the sealing being performed by a transfer molding such that the resin member is provided as recited in the present claims, and advantages thereof; and other aspects of the present invention as discussed previously, and advantages thereof, as set forth in the foregoing.

In particular, note that in Glenn and in Lee, et al., the individual device substrates are provided very close to each other in the matrix of the plurality of device substrates. See, for example, Fig. 7A of Glenn; note also Fig. 3 of Lee, et al. It is respectfully submitted that the teachings of Glenn and of Lee, et al. would have

taught away from the sealing technique as in the present invention, being performed by a transfer molding such that the resin member is provided from one of the longer sides via plural flow gates, as in the present claims, much less wherein the resin member is provided from one of the longer sides to a location among a respective group of chip mounting areas, and distributed therefrom to each chip mounting area of the respective group of chip mounting areas, as in various of the present claims.

In view of the foregoing comments and amendments, reconsideration and allowance of all claims presently in the application are respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.36384CC9) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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